CBCS SCHEME

USN | | | | | | | | | | |

15ELN15/25

First/Second Semester B.E. Degree Examination, Dec.2019/Jan.2020
Basic Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What is Rectifier? Explain the operation of full wave rectifier, with neat circuit and waveform. **(06 Marks)**

b. Explain the operation of npn transistor. **(04 Marks)**

c. A half wave rectifier circuit is supplied from secondary transform voltage of 108.423V to a resistive load of 10KΩ. The diode forward resistance is 10Ω. Calculate the maximum , average , RMS value of current , DC output voltage , efficiency of transformer. **(06 Marks)**

OR

2 a. Explain the input and output characteristics of npn transistor in Common Base Mode. **(06 Marks)**

b. Draw the V- I, characteristics of Si and G_e diode. **(04 Marks)**

c. Establish the relationship between α and β. Also calculate β, α and I_E of the transistor, when I_B = 100μA and I_C = 2mA. Find new value of B when I_B changes by +25 μA and I_C by 0.6mA. **(06 Marks)**

Module-2

3 a. Define the following and derive the expression for its output voltage
i) Differentiator ii) Integrator. **(06 Marks)**

b. List the ideal characteristics of Op - amp. **(04 Marks)**

c. Calculate the minimum and maximum values of I_C and V_{CE} for the voltage divider bias circuit when $h_{fc(max)}$ = 60 and $h_{fc(min)}$ = 50. For circuit V_{CC} = 12V , R_1 = 10K , R_2 = 2K , R_E = 470Ω and R_C = 2K. Assume Silicon transistor. **(06 Marks)**

OR

4 a. For the circuit diagram shown in fig. Q4(a), Si transistor with β = 50 is used. Draw dc load line and determine the operating point. **(08 Marks)**

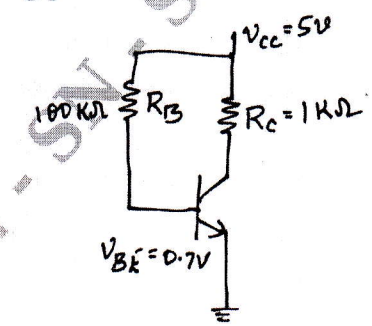

Fig.Q4(a)

b. Draw inverting bumming amplifier circuit and obtain an expression for the output voltage. **(06 Marks)**

c. Find the gain and output voltage for a non – inverting amplifier using Op – amp when input voltage is i) 0.5V ii) -3V. **(02 Marks)**

Module-3

5 a. State and prove De Morgan's Theorem for 3-variables. **(04 Marks)**

b. Realize the following expression using only NAND gates
$f = (A + \overline{B} + C)(\overline{A} + B + C)$. **(04 Marks)**

c. Explain full adder and implement full adder using two half adder and an OR gate. **(08 Marks)**

OR

6 a. Perform Binary subtraction using 1's and 2's complement method for the following :
i) 15 – 13 ii) 28 - 19. **(08 Marks)**

b. Convert the following : i) $(12.125)_{10} = (?)_2$ ii) $(10AB)_{16} = (?)_2$
iii) $(101010111100)_2 = (?)_{16}$ iv) $(57.6)_8 = (?)_2$. **(04 Marks)**

c. Realize OR and AND gates using only NAND gates and using only NOR gates. **(04 Marks)**

Module-4

7 a. Explain NOR gate latch. **(04 Marks)**

b. With neat block diagram, explain the architecture of micro controller. **(08 Marks)**

c. Explain the working of clocked RS flip flop. **(04 Marks)**

OR

8 a. List the difference between Microcontroller and Microprocessor. **(04 Marks)**

b. With neat block diagram, explain the interfacing of stepper motor to 8051 microcontroller. **(08 Marks)**

c. Explain NAND gate latch. **(04 Marks)**

Module-5

9 a. Explain the need for modulation. **(04 Marks)**

b. An audio frequency signal 10 sin 2π 500t is used to amplitude modulate a carrier of 50 sin 2π 10^5. Calculate i) Modulation index ii) Side band frequencies
iii) Amplitude of each side band iv) Bandwidth required
v) Total power delivered to the load 600Ω vi) Transmission efficiency. **(06 Marks)**

c. Give the comparison between FM and AM. **(06 Marks)**

OR

10 a. Explain the working of Envelope detector. **(04 Marks)**

b. Define Modulation index in terms of E_{max} and E_{min}. **(06 Marks)**

c. Write short note on :
i) Resistive transducer ii) Peltier effect iii) Seebeck effect. **(06 Marks)**

* * * * *